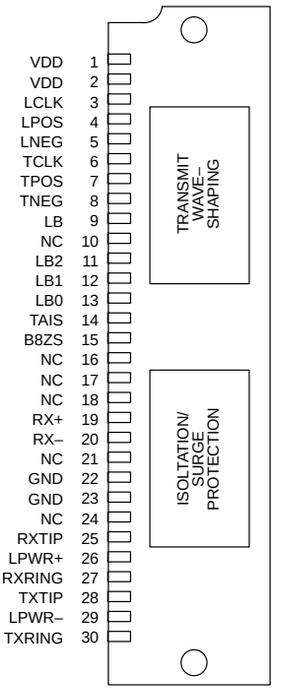
DALLAS SEMICONDUCTOR

DS2290
T1 Isolation Stik

FEATURES

- Protected interface for connecting equipment to T1 lines
- Provides 800 volts of surge protection and 1500 volts of isolation
- FCC Part 68 registered
- Meets TR 62411 and T1.403–1989 for transmit pulse characteristics
- Line build outs of 0, –7.5, and –15 dB
- Companion to the DS2291 T1 Long Loop Stik
- Connects to a standard 30–pin single in–line connector
- Single +5V supply
- Compatible with the DS2180A and DS2141A T1 Tranceivers

PIN ASSIGNMENT



(ACTUAL SIZE)

DESCRIPTION

The DS2290 T1 Isolation Stik provides all the surge and isolation protection that is necessary to connect a piece of equipment to a T1 line. It offers a function similar to that provided by a Data Access Arrangement (DAA) when a modem is connected to a phone line. The DS2290 is FCC Part 68 pre–registered so the user can connect equipment to T1 lines without any further testing or qualification. It contains onboard waveshaping circuitry that creates transmit pulses meeting the latest T1 specifications including TR 62411 (Accunet* T1.5 Service Description and Interface Specifications, – December 1990) and T1.403–1989 (Carrier to Carrier Installation – DS1 Metallic Interface). Applications include Channel Service Units and similar equipment that requires a fully protected interface.

* Service mark of AT&T Communications

OVERVIEW

The DS2290 contains all the isolation and surge protection required to connect equipment to T1 lines. The Isolation Stik has a receive and a transmit section. (See Figure 1.) In the receive section, inputs RXTIP and RXRING are connected directly to the receive T1 twisted pair. These inputs are terminated at 100 ohms. The T1 signal received at RXTIP and RXRING is coupled through a 2:1 transformer and presented at the RX+ and RX– outputs. See Figure 2. There is a full 1500 volts of isolation between the Network Side pins and the Customer Side pins.

In the transmit section, data that is to be transmitted is sourced from either the TPOS and TNEG inputs or the LPOS and LNEG inputs. The Data Mux will transmit data at the TCLK rate from the TPOS and TNEG inputs if the LB pin is either tied low or left open. It will transmit data at the LCLK rate from the LPOS and LNEG inputs if the LB pin is tied high. In order to comply with the latest T1 standards, the clock presented at either TCLK or LCLK must be at a 1.544 MHz rate (±32 ppm) and must not jitter beyond 0.05 unit intervals peak–to–peak (UIpp). TPOS and TNEG can be tied together if the source of the transmit data is in a NRZ format. The DS2290 will automatically sense that these inputs are tied together and will create a bipolar data stream from them. The same holds true for the LPOS and LNEG inputs.

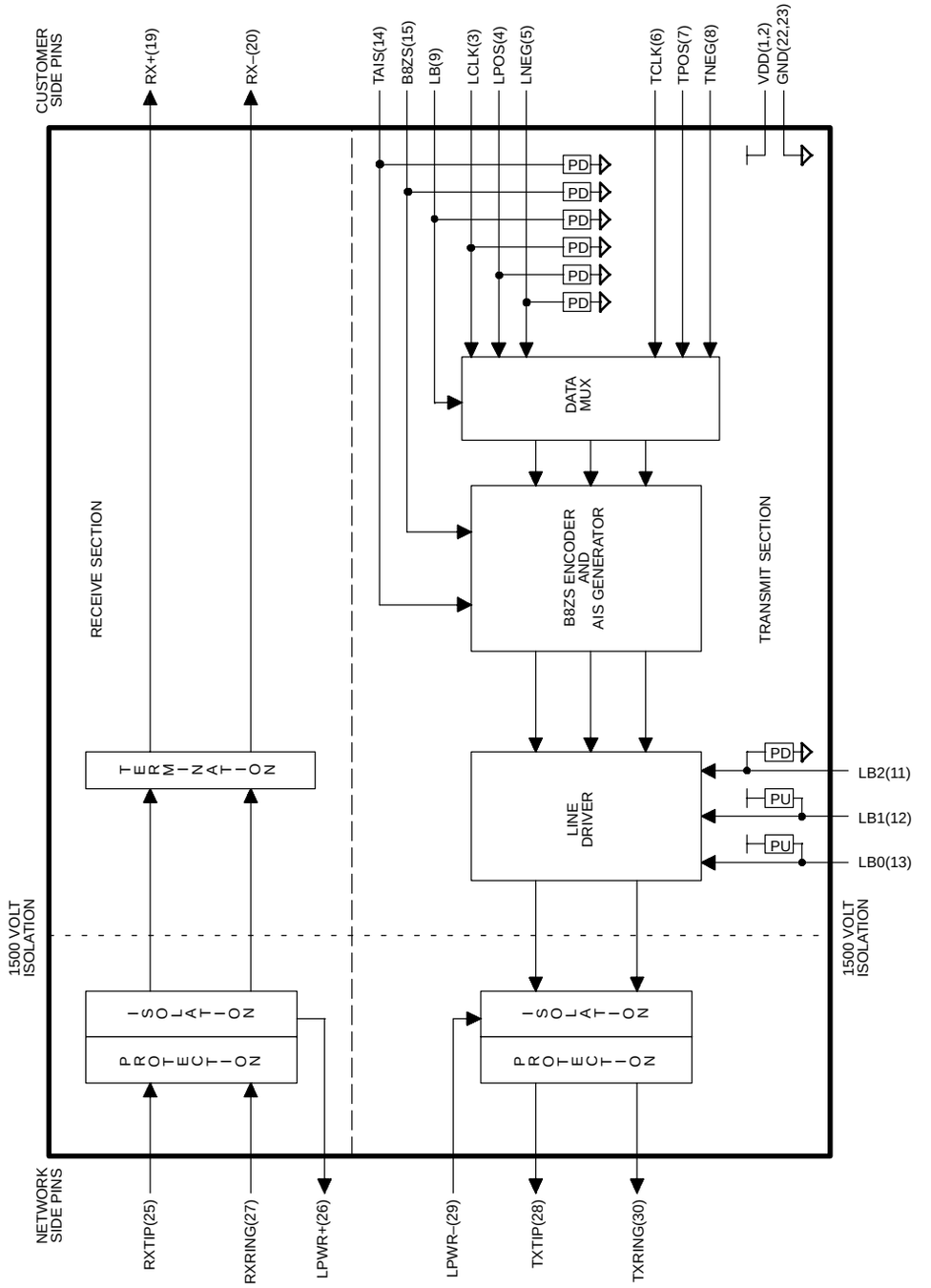
Data out of the Data Mux is passed to a B8ZS encoder and AIS generator. If the B8ZS pin is tied high, then the DS2290 will properly encode the transmit data stream for the B8ZS zero code suppression scheme. If the B8ZS pin is tied low or left open, the DS2290 will not encode the transmit data for B8ZS. Also, the DS2290 can be configured to transmit an AIS (Alarm Indication Signal). If the TAIS pin is tied high, the DS2290 will transmit an unframed, all ones signal at either the TCLK (LB=0) or LCLK (LB=1) rate.

The data to be transmitted is fed to the line driver. The line driver creates the T1 pulse that will be transmitted. The line build out pins LB0 to LB2 select whether the output pulse level will be 0, –7.5, or –15 dB (see Table 3). If 0 dB of build out is selected, the output pulse will conform to the shape described in Figure 2. This pulse shape is congruent with the latest T1 specifications such as TR 62411 and T1.403–1989. If the –7.5 dB or –15 dB line build outs are selected, then the pulse shown in Figure 3 will be attenuated according to the transfer function as described in FCC Part 68, Subpart D. Once the T1 pulse has been created, it is then transmitted onto the transmit T1 twisted pair via the TTIP and TRING outputs.

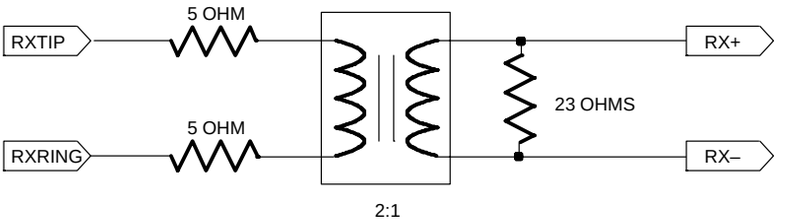
The DS2290 contains provisions for line powering. If the DS2290 is to be powered from the T1 line using a DC simplex power arrangement, then an external DC–to–DC converter can connected to the LPWR+ and LPWR– pins. Requirements for line powering are currently being relaxed and will be totally removed in the future. If the DS2290 is not line powered, the LPWR+ and LPWR– pins should be tied together.

Figure 4 shows a typical application using the DS2290. The transmit and receive T1 twisted pairs are connected directly to the DS2290. The DS2291 T1 Long Loop Stik recovers clock and data from the protected signal provided by the Isolation Stik. The DS2180A T1 Transceiver frames to the recovered data and interfaces to the system backplane. The DS2250 Soft Microcontroller Stik is used to control and monitor the status of the other devices.

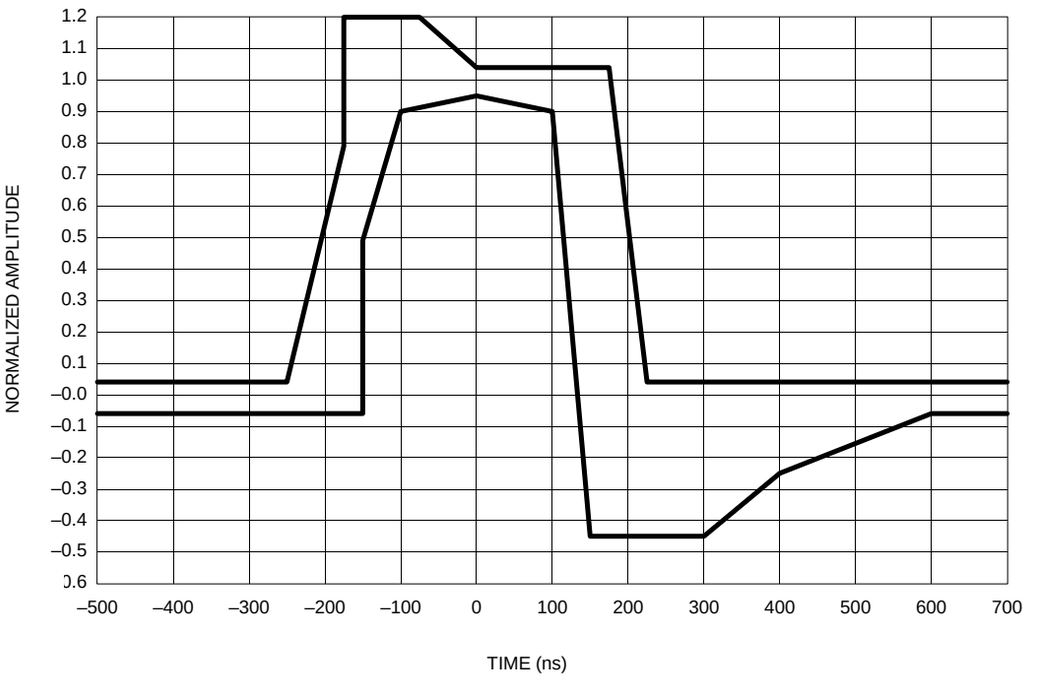
DS2290 BLOCK DIAGRAM Figure 1



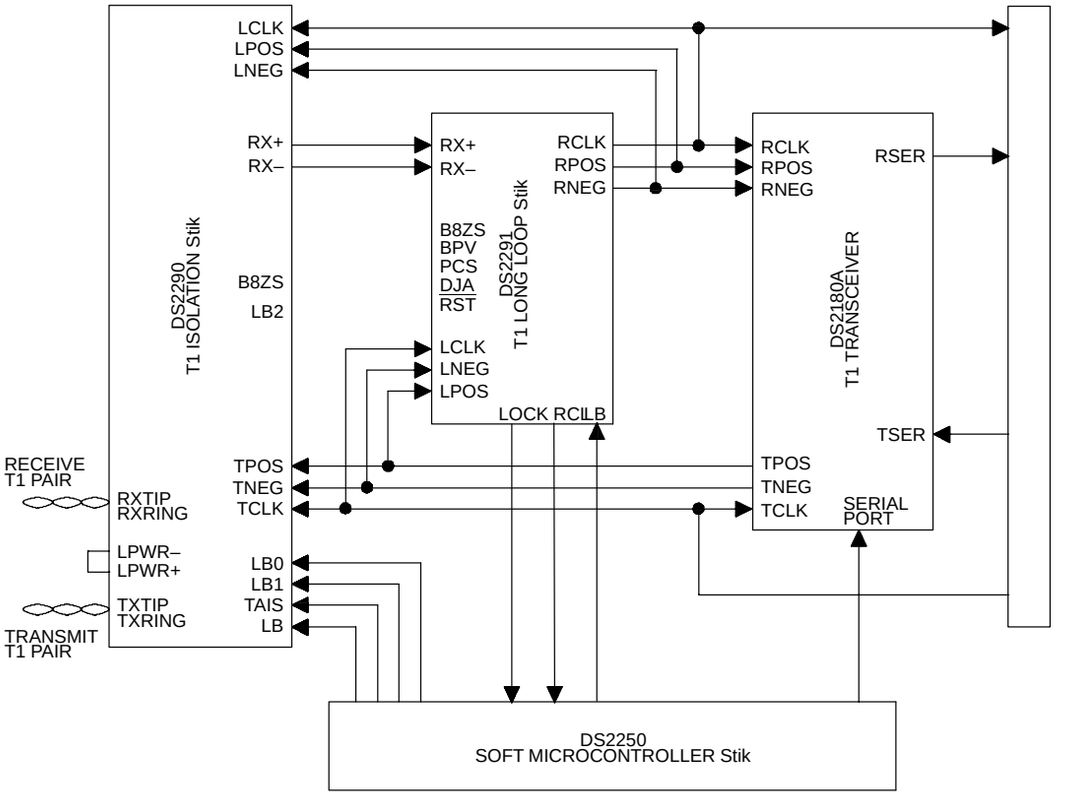
DS2290 RECEIVE SECTION CIRCUITRY Figure 2



OUTPUT PULSE TEMPLATE Figure 3



TYPICAL DS2290 APPLICATION Figure 4



NETWORK SIDE PIN DESCRIPTION Table 1

PIN	SYMBOL	I/O	DESCRIPTION
25 27	RXTIP RXRING	I	**Receive Tip and Ring Inputs.** Connects directly to the receive T1 twisted pair. These inputs are transformer coupled and terminated at 100 ohms. See Figure 2.
28 30	TXTIP TXRING	O	**Transmit Tip and Ring Outputs.** Connects directly to the transmit T1 twisted pair. Output signal level is programmable via the LB0 to LB2 pins. (See Table 3.)
26 29	LPWR+ LPWR–	–	**Loop Power Connections.** These pins connect to the internal center–taps of the transmit and receive transformers. They provide access to the DC power on the T1 line (may not be provided by carriers in the future). Tie together if no simplex power arrangement is needed.

CUSTOMER SIDE PIN DESCRIPTION Table 2

PIN	SYMBOL	I/O	DESCRIPTION
1,2	V_{DD}	–	**Positive Supply.** 5.0 Volts.
3	LCLK	I	**Loopback Clock.** Clock for loopback data. Internally pulled low by 100KΩ.
4 5	LPOS LNEG	I	**Loopback Bipolar Data.** Sampled on the falling edge of LCLK if LB is tied high. Internally pulled low by 100KΩ.
6	TCLK	I	**Transmit Clock.** Apply a 1.544 MHz (±32 ppm) clock here.
7 8	TPOS TNEG	I	**Transmit Bipolar Data.** Data that is to be transmitted. Sampled on the falling edge of TCLK when LB is tied low or left open. TPOS and TNEG can be tied together for an NRZ data input.
9	LB	I	**Loopback Enable.** Tie high to transmit data from LPOS and LNEG; tie low or leave open to transmit data from TPOS and TNEG. Internally pulled low by 100K ohm.
11 12 13	LB2 LB1 LB0	I	**Line Build Out Select.** State determines whether the transmitted signal has 0, –7.5, or –15 dB of line build out. See Table 3. LB0 and LB1 are internally pulled high by 100KΩ; LB2 is pulled low by 100KΩ. If all three build out pins are left open, the default state is 0 dB.
14	TAIS	I	**Transmit Alarm Indication Signal.** Tie high to transmit an unframed all ones signal at either the TCLK (LB=0) or LCLK (LB=1) rate. Internally pulled low by 100KΩ.
15	B8ZS	I	**B8ZS Enable.** Tie high to enable B8ZS encoding; tie low or leave open to disable B8ZS encoding. Internally pulled low by 100KΩ.
19 20	RX+ RX–	O	**Receive Analog Output.** Protected differential T1 signal output here.
22,23	GND	–	**Ground.** 0.0 volts.

NOTE: Do not connect any signal to pins 10, 16, 17, 18, 21, and 24.

LINE BUILD OUT SELECTS Table 3

LINE BUILD OUT SELECTS	LB0	LB1	LB2
0 dB	1	1	0
–7.5 dB	1	0	0
–15 dB	0	1	0

SINGLE IN–LINE CONNECTOR

The DS2290 is designed to connect directly into a 30–position single in–line connector. These connectors are available from a number of vendors.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground (Customer Side pins only)	–0.3V to V_{CC} + 0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	3
Logic 0	V_{IL}	–0.3		+0.8	V	3
Supply	V_{DD}	4.75		5.25	V	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Capacitance	C_{IN}		30		pF	3
Output Capacitance	C_{OUT}		50		pF	3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		60	80	mA	1
Input Leakage	I_I	–100		+100	µA	2,3
Output Current (2.4V)	I_{OH}	–1.0			mA	3
Output Current (0.4V)	I_{OL}	+4.0			mA	3

NOTES:

1. TCLK = 1.544 MHz; V_{DD} = 5.25V; outputs open; driving all ones into 6000 feet of 22 AWG.
2. $V_{SS} < V_{IN} < V_{DD}$.
3. Does not apply to any of the network side pins nor RX+ or RX–.

ANALOG ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Impedance at RXTIP and RXRING at 772 KHz	I_Z	95	100	105	ohms	1
Transmit Jitter Generation	J_{GEN}			0.03	UIpp	2
Transmit Pulse Amplitude	P_{AMP}	2.5	3.0	3.5	Vpk	3,4,5
Pulse Width Balance @ 50%	PW_{BAL}		1	10	ns	3,6
Pulse Amplitude Balance	PA_{BAL}		10	100	mV	3,6
Power Level at 772 KHz	P_{LVL}	12		19	dBm	7

NOTES:

1. RX+ and RX– left open circuited.
2. Jitter present at TXTIP and TXRING with no jitter at TCLK (LB=0) or LCLK (LB=1).
3. Measured with 100 ohm (±5%) termination at TXTIP and TXRING.
4. Measured directly at TXTIP and TXRING with 0 dB of line build out.
5. Pulse shape meets template in Figure 3 over temperature and voltage.
6. Measured over 17 consecutive pulses.
7. Measured in a 2 KHz to 3 KHz band about 772 KHz; power level in a 2 to 3 KHz band at 1.544 MHz is at least 25 dB lower.

DIGITAL ELECTRICAL CHARACTERISTICS

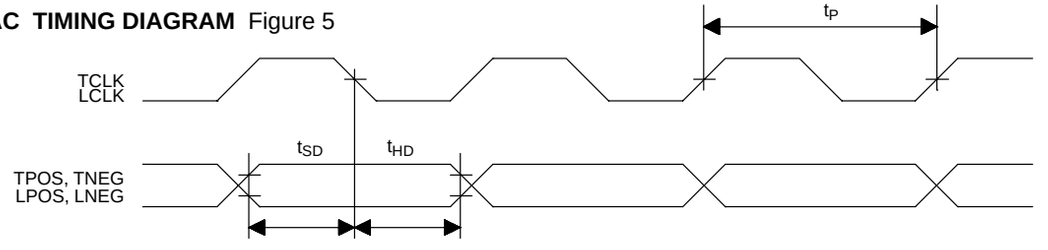
(0°C to 70°C; V_{DD}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_P			±32	ppm	1
TPOS, TNEG or LPOS, LNEG Setup Time to TCLK or LCLK Falling	t_{SD}	50			ns	
TPOS, TNEG or LPOS, LNEG Hold Time from TCLK or LCLK Falling	t_{HD}	50			ns	

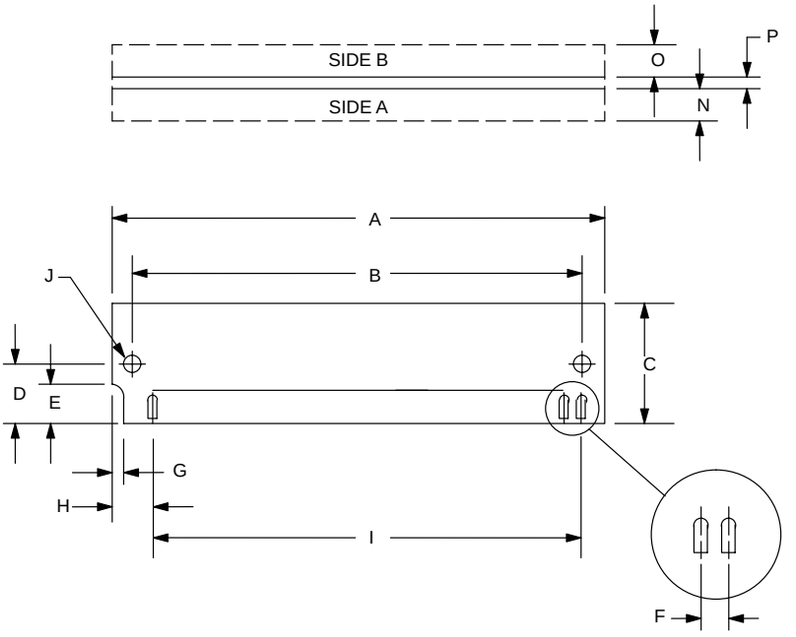
NOTE:

1. Necessary to meet current carrier and FCC specifications.

AC TIMING DIAGRAM Figure 5



DS2290 T1 ISOLATION Stik



PKG	30-PIN	
DIM	MIN	MAX
A IN.	3.455	3.505
B IN.	3.229	3.239
C IN.	0.845	0.855
D IN.	0.395	0.405
E IN.	0.245	0.255
F IN.	0.100 BSC	
G IN.	0.075	0.085
H IN.	0.295	0.305
I IN.	2.900 BSC	
J IN.	0.120	0.130
N IN.		0.235
O IN.		0.100
P IN.		0.054